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EXAMINER	
ABDULSELAM, ABBAS I	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,010	WILLIS, THOMAS E.	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on October 1, 2004. Claims 1-47 are pending.

Response to Arguments

2. Applicant's arguments filed on 10/01/04 have been fully considered but they are not persuasive.

Applicant argues that the cited references Chiu (USPN 6107979) and Buckelew et al. (USPN 6667744) alone or in combination do not teach a multi-pixel memory array that is physically decoupled from a multi pixel display array, and performing a digital function on a pixel data value and a counter value. However, as shown in the art rejection below, Buckelew teaches pixel storage method in which plane sets that affect the display area are physically separated from plane sets that do not affect the display area in order that a frame buffer is read to satisfy screen refresh requirements. See col. 18, lines 6-11. Buckelew clearly mentions storing display area separately and hence reads over the feature of the claim. Chiu teaches a device 10 being a digital micro mirror device (DMD) such that each micro mirrors comprise one pixel (see fig. 1). Chiu also teaches a data complementer circuit (56), which controls the pixel data transfer as true/false data as shown in Fig. 12 and Table 5. Chiu illustrates in Table 5 where the rows of memory array (14) can be alternately loaded with a logic "0" or a logic "1" by enabling or disabling the complement input (col. 14, lines 13-25).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Both Chiu and Buckelew teach displaying images and one of ordinary skill in the art would have looked toward Buckelew for the manner by which the memory functions.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 2, 10, 15, 21 and 26- 27, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al. (USPN 6107979) in view of Buckelew et al. (USPN 6667744).

Regarding Claim 1, 10, 15 and 21, Chiu teaches a monolithic spatial light modulator having a pixel array, which is programmable and may be implemented into a display system (col. 1, lines 26-31 and col. 3, lines 9-18). Referring to Fig.1, Chiu teaches a programmable format pixel array device (10) which includes 864x576 micro mirror array (12) where each of these micro mirrors comprise one pixel. Chiu teaches that a peripheral control circuitry and an underlying 864x36 array of memory cell (14) control these mirrors and provide on-chip programmable features including supporting four active array formats of the 864x576 DMD

mirror array. Chiu teaches a row address circuitry permitting all or less that all m pixels to be implemented in a display device. See col. 3, lines 19-26. Chiu also teaches a column data load circuitry further comprising means to selectively format loading of pixels to all or a subset of n pixel columns. As a result, Chiu teaches that unused number of pixels are automatically excluded and do not contribute to the display image (Fig. 2). See col. 3, lines 27-30. Chiu discloses a diagram of four pixel formats, which can be realized by the programmable pixel array (Fig. 2), and further indicates that a mirror array (12) is controlled by the memory array (14), whereby memory array is controlled by a programmable row addressing circuit (30) and a programmable column data loading/unloading circuit (32). See col. 7, lines 54-58. Chiu teaches that that the pixel array can be selectively formatted and the array device can be manufactured. See col. 3, lines 2-9. Specifically considering formats C, D of Fig. 2, Chiu teaches memory cells (14) and mirror array (12) of 640x480 pixel array such a logic "0" is written to all the memory cells (16) in rows MR0-MR2 and MR33-MR35 and data is written only to the memory cells of rows MR3-MR32 which is a total of 30 rows. Moreover, Chiu teaches that selections (C, D) of Fig. 2 is illustrated in Fig. 3 where a selection is controlled in hardware by simply establishing a logic "1" on logic line Vsize. See col. 7, lines 62-67 and Fig. 3. However, Chiu does not specifically teach the first and second areas belonging to pixel memory array and pixel display array respectively each coupled to a logic circuit such that the two areas are substantially non-overlapping. However as mentioned above, Chiu does teach a mirror array (12) which is controlled by the memory array (14), whereby memory array is controlled by a programmable row addressing circuit (30) and a programmable column data loading/unloading circuit (32).

It would have been obvious to utilize Chiu's the addressing circuit (30) and a programmable column data loading/unloading circuit (32) for the purpose of manipulating the size of a mirror array (12). One would have been motivated that in view of the suggestion that the programmable row addressing circuit (30) and the programmable column data loading/unloading circuit (32) can be used to modify Fig. 1 in order that memory array (14) does not substantially overlap with mirror array (12).

Regarding claim 21, in addition to what has been described above, Chiu teaches monolithic spatial light modulators having pixel arrays, which may be implemented in a display and particularly, teaches a universal pixel array with programmable active size. See col. 1, lines 26-31. Also see Fig. 3 where cells (20, 22) of memory array (14) are utilized. Chiu states that a single hardware programmable format pixel array is utilized to realize a functional pixel array with different dimensions of active pixels as a function of a single data entry. See col. 3, lines 38-42. Chiu teaches a data of secondary memory cell (22) configured with address electrodes (28, 29) as shown on Fig. 3. Furthermore, Chiu teaches a programmable column data loading and unloading circuit (32) and row addressing circuit (30) controlling memory array. It would have been obvious to utilize the circuit (30, 32) for the purpose of the desired comparison.

Chiu does not specifically teach counter value generating results, and in response either activating or deactivating a pixel cell. Chiu on the other hand teaches a data complementer circuit (56), which controls the pixel data transfer as true/false data as shown in Fig. 12 and Table 5. Chiu illustrates in Table 5 where the rows of memory array (14) can be alternately

loaded with a logic "0" or a logic "1" by enabling or disabling the complement input (col. 14, lines 13-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a data complementer circuit (56) for the purpose of controlling the status of the pixel data. One would have been motivated in view of the suggestion that the complementer circuit (56) equivalently provides the desired activating and deactivating of a pixel cell.

Chiu does not teach "a multi-pixel memory array that is physically decoupled from the multi-pixel display array." Buckelew on the other hand teaches pixel storage method in which plane sets that affect the display area are physically separated from plane sets that do not affect the display area in order that a frame buffer is read to satisfy screen refresh requirements. See col. 18, lines 6-11.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chiu's video display system to adapt Buckelew's pixel storage method. One would have been motivated in view of the suggestion in Buckelew that pixel storage method, expressed with respect to plane sets equivalently satisfies the desired separation of pixel memory from pixel display. The use of pixel-storage method helps display graphic images as taught by Buckelew.

Regarding claims 2 and 26-27, Chiu teaches a programmable column data loading and unloading circuit (32) and row addressing circuit (30) controlling memory array. It would have been obvious to utilize the circuit (30, 32) for the purpose disposing all of the pixels of the memory array outside the display area.

Claims 3-9, 11-14, 16-20, 22-25, and 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al., Buckelew et al. in further view of Miles (USPN 5986796).

Regarding claims 3, 11, and 16, Chiu as modified has been discussed above. However, Chiu does not teach, "at least one local width modulation drive circuit coupled to at least one of the pixel storage cells." Miles on the other hand teaches pulse width modulation signals being delivered from circuitry (26) to the pixel circuit modules (46) each circuit module (46) in the row including storages (180, 182). See Fig. 2 and Fig. 11.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Chiu's spatial light modulating system to adapt Miles' control circuitry (26) along with circuit modules (46). One would have been motivated in view of the suggestion in Miles that a control circuitry (26) and circuit modules (46) as configured in Fig. 2 and Fig. 11 are functionally equivalent to the desired width modulation driving circuit coupled to storage cells. The use of control circuitry (26) and circuit models (46) helps function modulator arrays as taught by Miles.

Moreover, Miles teaches a circuit model of Fig. 2 including a binary counter (320). See Fig. 11.

Regarding claim 4, Miles teaches a device (20) including screen (22) for displaying or sensing a high-resolution color image or a succession of color images under a control of power and control circuitry (26). See Fig. 4, lines 38-46

Regarding claims 5 and 7, Miles discloses using binary array to perform brightness control and the analog array to perform color selection allowing the generation of images with variable colors. See Fig. 23E and col. 18, lines 13-18.

Regarding claims 6, 12, 14, 17-18 and 22-24, Chiu teachers a micro mirror device (10) with more than one display format (col. 22, lines 64-67) and illustrates that the device (10) includes a counter (42). See Fig. 1. Chiu teaches a data of secondary memory cell (22) configured with address electrodes (28, 29) as shown on Fig. 3. In addition, Chiu teaches a programmable column data loading and unloading circuit (32) and row addressing circuit (30) controlling memory array. It would have been obvious to utilize the circuit (30, 32) for the purpose of the desired comparison.

Regarding claims 8-9, Miles teaches a full nine-pixel display including replications of the array of Fig. 23A illustrated in terms of separate color planes (610, 612, 614) each of which interacts only with and reflects one color from red green or blue. See col. 17, lines 55-65 and Fig. 23(A-B).

Regarding claims 13, 19-20 and 25, Chiu mentions gray scale of pixels forming an image is achieved by pulse width modulation techniques. See col. 2, lines 21-27.

Regarding claims 44-47, Chiu teaches a digital micro-mirror device (DMD) suitable for use in displays and projectors. Chiu teaches that the DMD is a monolithic single-chip integrated circuit spatial modulator (SLM) comprising micro mirrors fabricated over SRM cells and address electrodes. See col. 1, lines 58-67.

Claims 34-35 are rejected under 35 U.S.C. 103(a) being unpatentable over Chiu et al. (USPN 6107979) in Buckelew et al. and in further view of Takanashi et al. (USPN 5565882).

Regarding claim 34, Chiu as modified has been discusses above. However, Chiu does not teach the use of a polarization beam splitter included in the projection device. Takanashi on the other teaches a polarization beam splitter (924) in the image processing systems as shown in Fig. 11. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was to further modify Chiu's spatial light modulating system to adapt Takanashi's polarization beam splitter. One would have been motivated in view of the suggestion in Takanashi that the polarization beam splitter (924) as configured in Fig. 11 is equivalent to the desired polarization beam splitter. The use of a polarization beam splitter (924) helps function a spatial light modulator (922) as taught by Takanashi. Et al.

Regarding claim 35, Chiu teaches a display system in which a spatial light modulator is provided with respect to three areas of the picture (130). See Fig. 4.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Patrick Edouard**, can be reached at **(703) 308-6725.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

February, 18, 2005

XIAO WU
PRIMARY EXAMINER